



Classification of digital logical circuits using Conditional Random Fields and Support Vector Machines

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Background. Digital sketches (Figure 1.) are important medium of communication used in computer science and engineering. Our goal is to build a system that classifies them. One approach is using Conditional Random Fields because this algorithm takes into account context during the classification process. While this algorithm performs well for the recognition of two types of strokes (two-way classification), it does not produce good results when recognizing three types of strokes (three-way classification). We aim to improve the accuracy.

Approach. We introduce a second algorithm to our system – Support Vector Machine (SVM). Instead of using a three-way classification, we used a combination of two-way classifications (e.g. stage one: Gate-Nongate followed by stage two: Wire-Label). For all possible classifications we examined

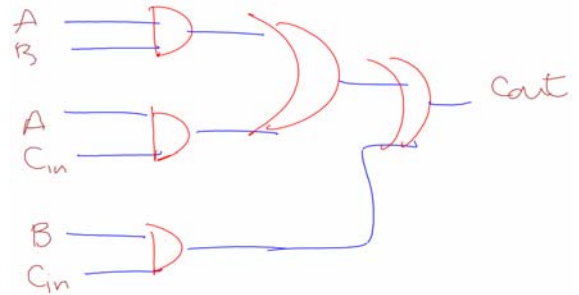


Figure 1. An example of a digital logical sketch.

which features of the strokes are most important for the recognition process. Another approach we explored is modifying the inference algorithm behind the CRF, namely Loopy Belief Propagation, so that we can tell it that certain strokes from the first stage of the classification are correctly labeled.

Results. The classification which produced the highest accuracy is Gate-Nongate (Figure 2) followed by Wire-Label (Figure 3). First we use the CRF to classify each stroke as a Gate or a Nongate, and then the SVM takes all the Nongate-s and classifies them as Wire-s or Label-s. The accuracy we obtained is as follows: Gate: 76.360%, Nongate: 83.146%, Wire: 84.800%, Label: 84.253% and overall accuracy of 72.142%.

Future Work. Implementing an inference algorithm alternative to Loopy Belief Propagation. This is necessary since there are some indications that it does not converge to the correct marginal probabilities because the graphs in the CRF contain loops.

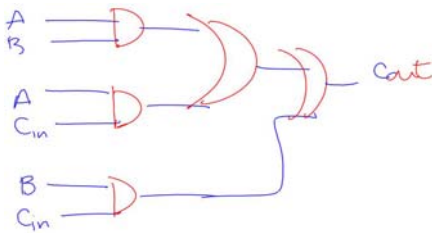


Figure 2. Gate-Nongate classification (CRF).

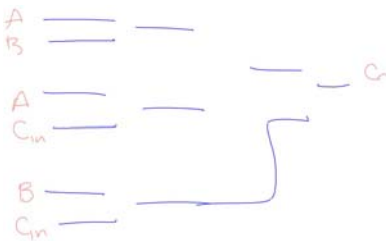


Figure 3. Wire-Label classification (SVM).

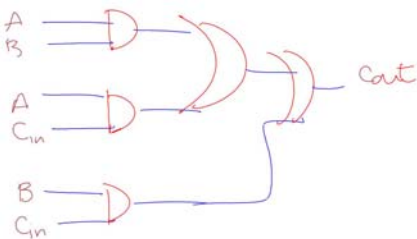


Figure 4. Final result.