

Electrical Engineering Pedagogical Software: A Circuit Simulator Graphical User Interface and Xilinx Bridge

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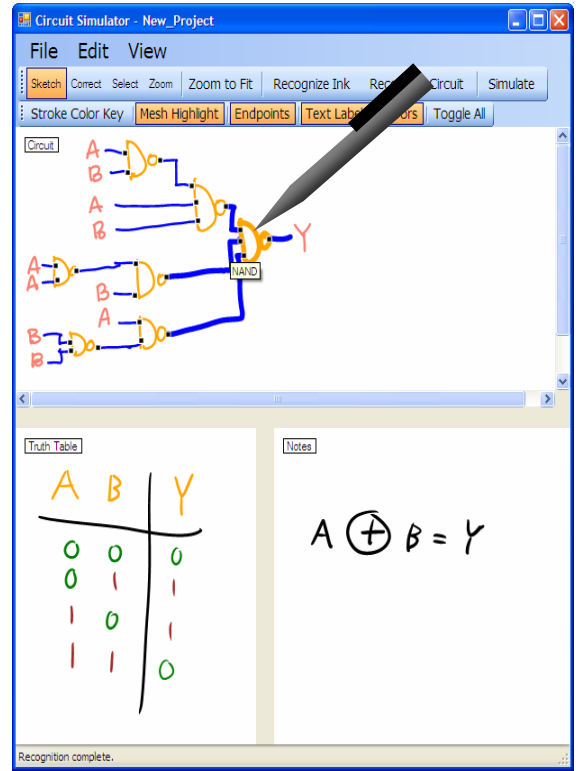
Background. Traditional mouse-and-keyboard-based computer aided design tools can be cumbersome to use. The Sketchers Research Group aims to build a complete sketch recognition system to provide a more natural procession from circuit design to simulation.

User Interface. Students draw directly on the screen of a Tablet PC or alternatively use a tablet input device. Students can load a designed circuit into the Xilinx Integrated Simulation Environment at the touch of a button. Built atop a sketch understanding engine developed at the Sketchers Research Group, the user interface color-codes recognized symbols and highlights connected and unconnected wire endpoints. The interface provides useful circuit debugging features, such as an intuitive labeling tool for correcting symbol recognition errors. Furthermore, Students can highlight a symbol and its connected neighbors (e.g., a wire mesh) by hovering the stylus over the diagram.

User-Driven Development. The opinions of over 20 Harvey Mudd Engineers have informed the interface's design. Three user studies based upon truth table tasks support our feature set selection and interaction paradigm design.

Xilinx and ModelSim Bridge. Circuit synthesis and simulation is handled by the Xilinx and Modelsim CAD utilities. In order to interface with these utilities, the Sketcher program first transforms recognized circuits into Verilog. The program also generates a circuit specific Verilog test bench. The Sketcher program then generates and executes custom TCL scripts to create a new Xilinx project file and to **add the generated Verilog modules**. Communication with Modelsim is accomplished through the use of custom .fdo scripts. These scripts specify the Verilog modules to be simulated, adjust simulation parameters and initiate the Modelsim simulation.

Future Work. Additional user studies and an overall system evaluation will inform future interface refinements.



Circuit Simulator showing sample recognition result and user interface features

```
#Xilinx Xtclsh script
#This script is automatically
generated
#by Workpath

cd {c:\new_project}
project open lab1_xx
cd {c:\new_project}
catch {xfile add led.v} msg
catch {xfile add test.v} msg
cd {c:\new_project}
catch {project save_as lab1_xx}
msg
project close
```

Sample TCL script for adding Verilog files to a Xilinx project

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User interface design informed by Harvey Mudd Computer Science Research

"Designing a Sketch Recognition Front-End: User Perception of Interface Elements." Paul Wais, Aaron Wolin and Christine Alvarado. In Proc. of Eurographics Workshop on Sketch-Based Interfaces and Modeling (SBIM). Riverside, CA. 2007.